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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AHMADI, MOHSEN	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,648	AMERICA ET AL.	
	Examiner	Art Unit	
	Mohsen Ahmadi	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/17/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claims 4 and 5 are objected to because of the following informalities: Claim 4 is a duplicate of claim 5. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US Pat. 2004/0214446) in view of Stojakovic et al (US Pat. 2005/0051820).

The present claim generally requires a method of forming an oxidized tantalum nitride hard mask for dual damascene processing, the method comprising providing a semiconductor wafer, the wafer comprising: a base dielectric layer, a cap layer overlying the base dielectric layer, a dielectric layer overlying the cap layer, one or more hard mask layer overlying the dielectric layer and a tantalum nitride layer overlying the hard mask layers, subjecting the tantalum nitride layer to an oxidation process to convert tantalum nitride layer to oxidized tantalum nitride (TaO_xN_x).

Regarding claim 1, Figure 1 of Kim et al. discloses a semiconductor wafer comprising a dielectric layer 105, a cap layer 110, overlying the base dielectric a

dielectric layer 112, overlying the cap layer a hard mask layer 114, overlying the dielectric layer and forming trench 116 (See page. 5, paragraph [0060-62]), a tantalum nitride layer 324 overlying the hard mask layer (See page. 8, paragraph [0086]).

Kim et al. discloses all of the claimed features as stated above except for forming a tantalum nitride layer overlying the hard mask layers and subjecting the tantalum nitride layer to an oxidation process to convert tantalum nitride layer to oxidized tantalum nitride (TaO_xN_x).

Stojakovic et al. discloses exposing a multiple hard mask layer such as a tantalum nitride layer to an oxidation process to convert the tantalum nitride layer to oxidized tantalum nitride layer (See page. 1, paragraph [0007]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the oxidation process for converting tantalum nitride layer to oxidize the tantalum nitride of Stojakovic et al., in the stack layers of Kim et al. for it's known benefit of providing a hard mask structure for etching. As both reference disclose hard mask structures, and each disclose the use of tantalum nitride or oxidized tantalum nitride as a hard mask, the substitution of one hard mask layer for another would have been *prima facie* obviousness. The use of a known hard mask oxidized tantalum nitride, for its known purpose is *prima facie* obviousness.

Regarding claim 2, Kim et al. discloses a metal conductor such as copper is planarized using chemical mechanical polishing (Page 6, 7 paragraph [0074]). Kim et

al. also discloses a conductive material such as copper has a low resistivity, which is a material of choice for sub-quarter-micron interconnect (See page 1, paragraph [0007]).

Regarding claims 3, 10 and 15 Kim et al. discloses a single dielectric material such as silicon oxycarbide 112 is deposited on layer 110 (page 5, paragraph [0061]).

Regarding claims 5, 11 and 16, Figure 1 of Kim et al. discloses the dielectric layers 110, 112 and 114 "stack-up", where the hybrid dielectric known as a multiple layer for processing.

Regarding claim 7, Kim et al. is relied upon as discussed above and disclose all of the claimed features as stated above except for the creating a patterned photoresist layer and etching the tantalum nitride layer prior to oxidation.

Stojakovic et al. discloses patterning a photoresist layer and etching the tantalum nitride layer prior to oxidation (See page. 2 paragraph [0011]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to pattern a photoresist layer and etch a tantalum nitride hard mask layer prior to oxidation, in light of the disclosure of Stojakovic et al. which teaches patterning and etching a tantalum nitride hard mask prior to oxidation. It would have been obvious to one of ordinary skill in the art to pattern and etch the hard mask of Kim et al. prior to the oxidation as discloses by Stojakovic et al. for it's known benefit of patterning and etching a hard mask. The transposition of process steps would be obvious in light of the disclosure of Stojakovic et al.

Regarding claim 8, Kim et al. discloses all of the claimed features as stated above except for creating a pattern of photoresist layer and etching the oxidized tantalum nitride layer after the oxidation process.

Stojakovic et al. discloses a patterning a photoresist layer and etching the oxidized tantalum nitride layer after the oxidation process (See page. 2 paragraph [0013]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to pattern a photoresist layer and etch the oxidized tantalum nitride hard mask layer after the oxidation, in light of the disclosure of Stojakovic et al. which teaches patterning and etching the oxidized tantalum nitride hard mask layer after the oxidation process. It would have been obvious to one of ordinary skill in the art to pattern and etch the hard mask of Kim et al. after the oxidation as discloses by Stojakovic et al. for it's known benefit of patterning and etching a hard mask. The transposition of process steps would be obvious in light of the disclosure of Stojakovic et al.

Regarding claim 9, Figure 3D of Kim et al. discloses a dual-damascene method of processing a semiconductor wafer comprising a base dielectric layer 305 having circuit elements and planarized flush with the surface thereof to which a subsequent electrical connection is to be made (See page. 8 paragraph [0087]), forming a cap layer 310 over the base dielectric layer 305 and circuit elements, forming a dielectric layer 312 over the cap layer 310 and forming a first hard mask layer (HM1) 322 over the

dielectric layer 312 and forming a tantalum nitride layer 324 over the hard mask layer (See page. 7 paragraph [0078, 79, 83 and 86]) and lithographically etching the tantalum nitride layer to form trench opening (See figure. 1).

Kim et al. discloses all of the claimed features as stated above except for forming a second hard mask layer (HM2) over the first hard mask layer and etched tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer.

Stojakovic et al. discloses a method of forming a second hard mask layer (HM2) over the first hard mask layer and forming a tantalum nitride layer over the second hard mask layer and etched tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer. Stojakovic et al. discloses a hard mask may comprises one or more layers made from titanium, tantalum, tantalum nitride, titanium nitride, titanium oxide, tantalum oxide, or any combination thereof, for example. As one example, the hard mask may include a tantalum nitride layer, a titanium layer over the tantalum nitride layer, and a titanium nitride layer over the titanium layer. (See page. 1 paragraph [0007]). Also see figure. 5

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the first and second hard mask layer and forming tantalum nitride layer over the second hard mask layer and etch tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer of Stojakovic et al. in the process of Kim et al. for it's known benefit of forming a hard mask layer and etching a tantalum nitride to an oxidation process to form an oxidized tantalum nitride layer. As both reference disclose

hard mask structures, and each disclose the use of tantalum nitride or oxidized tantalum nitride as a hard mask, the substitution of one hard mask layer for another would have been *prima facie* obviousness. The use of a known hard mask oxidized tantalum nitride for its known purpose is *prima facie* obviousness. The use of multiple hard mask layer is obvious in light of Stojakovic et al. which teaches to use multiple hard mask layer.

Regarding claim 14, Figure 3D of Kim et al. discloses a dual-damascene method of processing a semiconductor wafer comprising a base dielectric layer 305 having circuit elements and planarized flush with the surface thereof to which a subsequent electrical connection is to be made (See page. 8 paragraph [0087]), forming a cap layer 310 over the base dielectric layer 305 and circuit elements, forming a dielectric layer 312 over the cap layer 310 and forming a first hard mask layer (HM1) 322 over the dielectric layer 312 and lithographically etching the oxidized tantalum nitride layer to form trench opening (See figure. 1).

Kim et al. discloses all of the claimed features as stated above except for forming a second hard mask layer (HM2) over the first hard mask layer and subjecting the tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer.

Stojakovic et al. discloses a method of forming a second hard mask layer (HM2) over the first hard mask layer and forming a tantalum nitride layer over the second hard mask layer and subjecting the tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer. Stojakovic et al. also discloses a hard mask may comprises one or more layers made from titanium, tantalum, tantalum nitride, titanium

nitride, titanium oxide, tantalum oxide, or any combination thereof, for example. As one example, the hard mask may include a tantalum nitride layer, a titanium layer over the tantalum nitride layer, and a titanium nitride layer over the titanium layer. (See page. 1 paragraph [0007]). Also see figure. 5

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the first and second hard mask layers and forming a tantalum nitride layer over the second hard mask layer and subjecting the tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer of Stojakovic et al. in the process of Kim et al. for it's known benefit of forming a hard mask layer and oxidizing tantalum nitride layer and etching the oxidized tantalum nitride layer to form trench. As both reference disclose hard mask structures, and each disclose the use of tantalum nitride or oxidized tantalum nitride as a hard mask, the substitution of one hard mask layer for another would have been *prima facie* obviousness. The use of a known hard mask oxidized tantalum nitride for its known purpose is *prima facie* obviousness. The use of multiple hard mask layers is obvious in light of Stojakovic et al., which teaches to use multiple hard mask layers.

Claims 6, 12, 13, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US Pat. 2004/0214446) in view of Stojakovic et al (US Pat. 2005/0051820) further in view of Narwankar et al. (US Pat. 2003/0025146).

Regarding claim 6, 12, 13, 17 and 18, Kim et al. and Stojakovic et al. are relied upon as discussed above and disclose all of the claimed features as stated above

except for the combined thermal and plasma oxidation process and where oxidation process comprises an oxidation environment with a N_2O flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr, a wafer substrate temperature between 250 degrees C and 400 degree C, a plasma power between 250 Watts and 1000 Watts.

Narwankar et al. discloses a thermal and plasma oxidation process (See page. 6 paragraph [0080]). Narwankar et al. also discloses a method wherein the oxidation process further comprises: an oxidation environment with a N_2O flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr (See page. 6 paragraph [0080]); a wafer substrate temperature between 250 degrees C and 400 degree C (See page. 4 paragraph [0063]); a plasma power between 250 Watts and 1000 Watts (See page. 5 paragraph [0063].

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the thermal and plasma oxidation process of Narwankar et al. in the oxidation of the tantalum nitride of Kim et al. and Stojakovic et al. for it's known benefit as an oxidation process, oxidizing tantalum nitride layer to oxidized tantalum nitride. As both references are drawn to the oxidation process using thermal and plasma oxidation process a *prima facie* case of obviousness is established.

Regarding claims 13 and 18, Narwankar et al. discloses a method wherein the oxidation process further comprises: an oxidation environment with a N_2O flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr (See page.

6 paragraph [0080]); a wafer substrate temperature between 250 degrees C and 400 degree C (See page. 4 paragraph [0063]); a plasma power between 250 Watts and 1000 Watts (See page. 5 paragraph [0063]. According to Narwankar et al. these parameters can be adjusted, however, on the basis of empirical results, if required, to yield optimum results.

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the oxidation environment with a N_2O flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr and the wafer substrate temperature between 250 degrees C and 400 degree C and the plasma power between 250 Watts and 1000 Watts of Narwankar et al. in the oxidation of the tantalum nitride of Kim et al. and Stojakovic et al. for their known benefit as an oxidation process of tantalum nitride by thermal and plasma oxidation process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsen Ahmadi whose telephone number is 1-571-272-5062. The examiner can normally be reached on Mon-Fri 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 1-571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MA

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER